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PATENT APPLICATION

A CHARACTERISTIC IMPEDANCE EQUALIZER AND AN INTEGRATED CIRCUIT PACKAGE EMPLOYING THE SAME

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TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to integrated circuit packaging and, more specifically, to a characteristic impedance equalizer and an integrated circuit package employing the same.

BACKGROUND OF THE INVENTION

[0002] Reliable operation of electronic devices, especially semiconductor devices, is of a primary importance today. Often the success of a company may depend on the success at which new technology is reliably established, especially in a developing market. Particularly challenging is the general market demand for devices that perform more functions at increasingly faster operating speeds. This demand for increased functionality usually drives the device design toward more complexity, which typically involves higher component densities. Higher densities alone complicate the environment for signal transmissions within the device. The demand for faster signal speeds further exacerbates

this condition causing the environments and associated designs that were acceptable at slower signal speeds to cross into the realm of unacceptability.

[0003] Signal environments that exist in a semiconductor die may require special attention to insure that the ever closer proximity of signals will not generate cross-talk or other interference conditions. Although challenging, these on-chip detrimental conditions may be overcome through appropriate layout and shielding designs. High speed, high density packaging substrate design, however, typically involves a constant trade-off between cost and electrical signal integrity requirements. To reduce costs, signals are often routed in a microstrip construction where the signal only references one power or ground plane.

[0004] Additionally, the construction of a flip chip package, for example, employs a copper stiffener to reduce warpage and a copper heatsink or slug to dissipate heat from the back of the semiconductor die. When a four-layer flip chip packaging substrate is used in this assembly configuration, the traces routed on the top layer are subject to several discontinuities in the electrical environment. One source of discontinuity is the microstrip trace routing from the central cavity area formed under the heatsink and the region under the stiffener. These discontinuities lead to a variation in the characteristic impedance associated with the

microstrip traces. This causes reflected noise and losses during signal transmission.

[0005] The discontinuity could be eliminated by using a strip line construction wherein the signal is sandwiched between power and ground planes for its entire length. However, this would need additional layers in the packaging substrate thereby increasing the cost. Another approach is to shrink the stiffener opening to bring it closer to an edge of the semiconductor die thereby providing a more uniform and controlled electrical environment for the microstrip traces on the top layer of the packaging substrate. However, this means different stiffener openings for every semiconductor die size. The resultant non-standardization in stiffener opening complicates the overall assembly process and thereby also increase assembly costs.

[0006] Accordingly, what is needed in the art is a way to provide a more controlled characteristic impedance that is both robust and cost effective in an integrated circuit package.

SUMMARY OF THE INVENTION

[0007] To address the above-discussed deficiencies of the prior art, the present invention provides a characteristic impedance equalizer for use with an integrated circuit package having first and second signal transmission zones. In one embodiment, the characteristic impedance equalizer includes a first conductor having a first width and providing a characteristic impedance within the first signal transmission zone. The characteristic impedance equalizer also includes a second conductor, coupled to the first conductor, having a second width and providing substantially the same characteristic impedance within the second signal transmission zone.

[0008] In another aspect, the present invention provides a method of manufacturing an integrated circuit package. The method of manufacturing includes providing a substrate configured to be partitioned into first and second signal transmission zones. The method further includes forming a first conductor having a first width and providing a characteristic impedance within the first signal transmission zone and forming a second conductor having a second width and providing substantially the same characteristic impedance within the second signal transmission zone.

[0009] In yet another aspect, the present invention provides an integrated circuit package that includes a substrate configured to be partitioned into first and second signal transmission zones. The integrated circuit package also includes a characteristic impedance equalizer with a first conductor having a first width providing a characteristic impedance within the first signal transmission zone and a second conductor having a second width providing substantially the same characteristic impedance within the second signal transmission zone.

[0010] The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0012] FIGURE 1 illustrates a side view of an embodiment of an integrated circuit package, constructed in accordance with the principles of the present invention;

[0013] FIGURE 2 illustrates a plan view of an embodiment of portions of an integrated circuit package including a substrate showing a surface portion that is proximate a metallic heatspreader and a metallic stiffener, constructed in accordance with the principles of the present invention;

[0014] FIGURE 3 illustrates a plan view of an embodiment of a portion of a substrate showing a plurality of conductors forming a portion of characteristic impedance equalizers, constructed in accordance with the principles of the present invention;

[0015] FIGURE 4 illustrates a plan view of an embodiment of a portion of a plurality of characteristic impedance equalizers showing a conductor transition area between two signal transmission zones, constructed in accordance with the principles of the present invention.

DETAILED DESCRIPTION

[0016] Referring initially to FIGURE 1, illustrated is a side view of an embodiment of an integrated circuit package, generally designated 100, constructed in accordance with the principles of the present invention. The integrated circuit package 100 includes a four-layer, flip chip substrate 105, an integrated circuit die 110, a metallic stiffener 115, a metallic heatspreader 120, a first signal transmission zone 125 and a second signal transmission zone 130.

[0017] The integrated circuit die 110 is positioned in the central area of the integrated circuit package 100 and is electrically coupled to the four-layer, flip chip substrate 105. Further, the integrated circuit die 110 is mechanically coupled between the four-layer, flip chip substrate 105 and the metallic heatspreader 120. In the illustrated embodiment, both the metallic stiffener 115 and the metallic heatspreader 120 are constructed of copper, which has an appropriate stiffness and provides good heat conductivity.

[0018] The metallic stiffener 115 is approximately square in cross-sectional area and formed of a single sheet of copper that has a square portion of its center section removed. The integrated circuit die 110 is placed in the center of this removed area, as

shown. Both the integrated circuit die 110 and the metallic stiffener 115 are bonded between the four-layer, flip chip substrate 105 and the metallic heatspreader 120. The metallic stiffener 115 and the metallic heatspreaader 120 cooperate to stiffen the overall package and remove the heat generated by the integrated circuit die 110.

[0019] This packaging regime produces the first and second signal transmission zones 125, 130. The first transmission zone 125 occurs between the four-layer, flip chip substrate 105 and the metallic heatspreader 120, and the second signal transmission zone 130 occurs between the four-layer, flip chip substrate 105 and the metallic stiffener 115. The first and second signal transmission zones 125, 130 create different signal transmission environments and properties due to the different nature of their respective proximity to the surface of the four-layer, flip chip substrate 105. In particular, the first and second signal transmission zones 125, 130 typically have different characteristic impedances for a conductor having a uniform width on the surface of the four-layer, flip chip substrate 105.

[0020] An embodiment of a method of manufacturing the integrated circuit package 100 includes providing the substrate 105 configured to be partitioned into first and second signal transmission zones 125, 130. A first conductor having a first

width and providing a characteristic impedance within the first signal transmission zone 125 and a second conductor having a second width and providing substantially the same characteristic impedance within the second signal transmission zone 130 are formed on the substrate 105. A junction (see FIGURE 4) between the first conductor and the second conductor is formed having a semi-circular cross-sectional area wherein the first width is greater than the second width. A plurality of the first and second conductors having appropriate junctions are formed on the substrate 105. Each of the first and second conductors provides a transmission path for a signal transmission.

[0021] The metallic stiffener 115 is positioned over a portion of the substrate 105 containing the second conductors to form the second signal transmission zone 130. The metallic heatspreader 120 is positioned over a portion of the substrate 105 containing the first conductors to form the first signal transmission zone 125 and over the metallic stiffener 115.

[0022] As will be discussed in more detail with respect to FIGURE 2, the top layer of the four-layer, flip chip substrate 105 may contain a plurality of conductors. These conductors traverse the first and second signal transmission zones 125, 130 and provide a plurality of signal transmission paths. In the illustrated embodiment, the four-layer, flip chip substrate 105 is configured

to be partitioned into the first and second signal transmission zones 125, 130. A characteristic impedance equalizer is employed in each of the conductors. Of course, an alternative embodiment of the present invention may employ an integrated circuit package having more than two signal transmission zones. Such an embodiment includes a characteristic impedance equalizer associated with each of the conductors that appropriately accommodates each signal transmission zone.

[0023] Turning now to FIGURE 2, illustrated is a plan view of an embodiment of portions of an integrated circuit package including a substrate, generally designated 200, showing a surface portion that is proximate a metallic heatspreader and a metallic stiffener, constructed in accordance with the principles of the present invention. The substrate 200 may be representative of the four-layer, flip chip substrate 105 as discussed with respect to FIGURE 1. The substrate 200 accommodates a plurality of conductors, collectively designated 205, that support a plurality of signal transmissions between a centrally-located integrated circuit die 210 and an outside perimeter 215 of the substrate 200. The substrate 200 also accommodates first and second signal transmission zones 220, 225.

[0024] Similar to FIGURE 1, the first signal transmission zone 220 is provided between a portion of the substrate 200 containing

a plurality of first conductors that are proximate the metallic heatspreader. The second signal transmission zone 225 is provided between a portion of the substrate 200 containing a plurality of second conductors that are proximate the metallic stiffener. In the illustrated embodiment, the respective thicknesses of the first and second conductors are essentially equal and configured to be much less than their respective first and second widths. In the illustrated embodiment, the first width is greater than the second width as will be further discussed with respect to FIGURE 3 below.

[0025] Each of the plurality of conductor transmission paths 205 employs a characteristic impedance equalizer that substantially matches a characteristic impedance between the first and second signal transmission zones 220, 225. The characteristic impedance equalizer includes the first conductor having the wider first width, which provides a characteristic impedance within the first signal transmission zone 220. The characteristic impedance equalizer also includes the second conductor, coupled to the first conductor and having the narrower second width, which provides substantially the same characteristic impedance within the second signal transmission zone 225.

[0026] Turning now to FIGURE 3, illustrated is a plan view of an embodiment of a portion of a substrate, generally designated 300, showing a plurality of conductors forming a portion of

characteristic impedance equalizers constructed in accordance with the principles of the present invention. The substrate 300 is partitioned into a first signal transmission zone 305 located approximately between an integrated circuit die boundary 315 and a metallic stiffener boundary 320. The substrate 300 is also partitioned into a second signal transmission zone 310 located approximately between the metallic stiffener boundary 320 and an outside perimeter of the substrate 300, which is not shown in FIGURE 3.

[0027] As may be seen in the embodiment of FIGURE 3, a characteristic impedance equalizer 303, which is typical of those employed in each of the plurality of conductors, transitions between a wider-width trace 325 and a narrower-width trace 330 in the vicinity of the metallic stiffener boundary 320. The wider-width trace 325 is located in the first signal transmission zone 305 to achieve a required characteristic impedance for signals traversing this portion of an overall transmission path between an integrated circuit die and a perimeter of the substrate 300. Similarly, the narrower-width trace 330 is located in the second signal transmission zone 310 to achieve substantially the same characteristic impedance of the first signal transmission zone 305.

[0028] The wider-width trace 325 is about 40 percent wider than the narrower-width trace 330, in the illustrated embodiment. This

value was determined from experimentation and simulation to provide a characteristic impedance equalizer that performs satisfactorily in achieving substantially the same characteristic impedance in the first and second signal transmission zones 305, 310. In the illustrated embodiment, all of the wider-width traces are of approximately equal widths. Similarly, all of the narrower-width traces are of approximately equal widths, as well.

[0029] In alternative embodiments of the present invention, the wider-width traces may employ more than one width, as may the narrower-width traces, to achieve a required characteristic impedance in different signal transmission zones. Additionally, a characteristic impedance equalizer may also employ more than the two trace widths of the illustrated embodiment to substantially maintain a characteristic impedance wherein two or more signal transmission zones are encountered.

[0030] Turning now to FIGURE 4, illustrated is a plan view of an embodiment of a portion of a plurality of characteristic impedance equalizers showing a conductor transition area between two signal transmission zones, constructed in accordance with the principles of the present invention. The conductor transition area includes a plurality of junctions, wherein a junction 405 is representative, between a first conductor 410 and a second conductor 415. In the illustrated embodiment, the junction 405 has a semi-circular cross-

sectional area as it transitions from the first conductor 410 to the second conductor 415. Alternatively, other embodiments of the junction 405 may employ other shapes or configurations that enhance an appropriate transition between the two signal transmission zones to maintain a substantially constant overall characteristic impedance.

[0031] In summary, several embodiments of a characteristic impedance equalizer for use with an integrated circuit package have been presented. Each of these embodiments of the present invention maintains the characteristic impedance at a substantially constant value for a transmission signal that traverses at least two different signal transmission zones. Maintaining a substantially constant characteristic impedance significantly reduces reflective signal energy along a transmission path and also reduces crosstalk energy between different transmission paths thereby enhancing overall performance.

[0032] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.